12V and 5V are located on the lower board of the power supply.

3.4.1 POWER SUPPLY USAGE

System Power Usage:	345 VA
BTU per hour:	700

The power supply has the following ratings:

Volts	Amps	
+ 5	25	
+12	4	
+24	2	(4 amps with semi-regulation)
-12	4	

Peripheral power usage:	+5V Amps	+12V Amps	+24V Amps
Winchester type disc drive	1.0	2.0	
Formatter	2.0	0.05	
Slimline floppy (each)	1.0		0.5
Tape drive	3.5		1.7

Backplane power usage:		+5V Amps	+12V Amps
CPU	LSI 11/23	2.0	0.2
Memory	SV128	2.0	0
Floppy/Tape Controller	XCV21 or CCV11	2.5	0
5 1/4-in. Winchester Controller	FCV21B	2.5	0
4 line serial Interface	DLV11J	1.5	0.25
Multifunction	MFV11	2.2	0.20
	TOTAL USED:	12.4	0.65

Power remaining in amperes for spare slots in backplane:

System	+ 5V	+12V
6210	12.5	3.35
6220/6221	8.0	1.30
6230/6231	7.0	1.30
6240/6241	5.5	1.30

Table 3-2. Modes of Operation

Operation Mnemonic	BDIN	BDOUT	BDAL00	BWTBT	Function
DATI	1	0	0	0	Read word from memory
DATIO	1	1	0	0	Read word from memory followed by a write word Read - modify - write
DATIOB	1	1	X	1	Read word from memory followed by a write byte Read - modify - write
DATO	0	1	0	1	Write word to memory
DATOB	0	1	X	1	Write byte to memory

X = signal could either true or false
0 = signal is false
1 = signal is true

Note

Signals BDIN and BDOUT are both true for a DATIO and DATOB operation, but not at the same time during the cycle.

Signal BWTBT is true at the beginning of both the DATO and DATOB operation. If a write word operation (DATO), BWTBT is negated at least 100 nanoseconds after BSYNC is asserted. If a write byte (DATO), BWTBT remains asserted.

3.5.3 REFRESH CYCLE

The PM-SV128 memory was designed using 64K dynamic MOS RAMs. Being dynamic, these memories require refreshing. Refresh cycles are controlled by the refresh logic contained on the memory. Refresh cycles occur at a periodic rate of approximately every 16 microseconds. The entire memory is refreshed every 4.096 milliseconds.

3.5.4 PARITY CONTROLLER

The PM-SV128 memory contains an on-board parity controller that is compatible with the Plessey PM-7850 and DEC M7850 parity controller. The on-board parity controller frees a dual-wide backplane slot for additional user expansion. The parity controller provides all parity generation and checking functions.

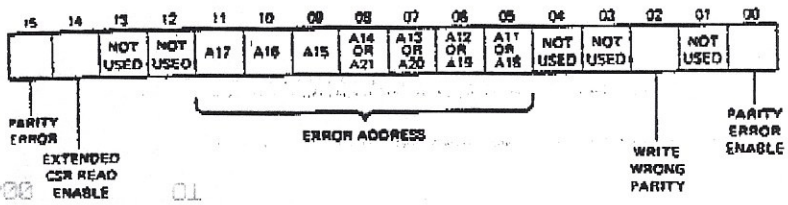
3.5.4.1 Control and Status Register

The control and status register in the PM-SV128 memory module contains bits that are used to store the parity error and address bits.

Bit 0 — When set, enables parity errors to trap and interrupt the CPU.

Bit 2 — When set, causes wrong parity to be written. This is a useful tool for checking the parity logic.

The CSR allows programs control of certain parity functions and contains diagnostic information. If a parity error has occurred. The CSR is assigned an address and may be accessed by a bus master via the LSI-11 Bus. Some CSR bits are cleared by assertion of BUS INIT L. This signal is asserted for a short time by the processor after system power has come up, or in response to a reset instruction. The CSR bit assignments are shown in the following diagram. Each bit assignment is explained.



Bit	Description
1,3,4,12,13	Not used.
0	Parity Error Enable. If set, and a parity error occurs on a DATI or DATIO(B) cycle to memory, then BDAL 16(L) and BDAL 17(L) are asserted on the bus at the same time as the data. This bit is read/write

and is reset to zero on power-up or BUS INIT.

2 Write Wrong Parity. If this bit is set during a DATO or DATOB cycle to memory, wrong parity data will be written into the parity MOS RAMs. This bit may be used to check the parity error logic as well as failed address information in the CSR. The following diagnostic is applicable:

1. With bit 2 set, write entire memory with any pattern.

2. Read first location in memory. If bit 0 of the CSR is set, then a parity error should be detected on the LSI Bus and the failed address at location (0) is stored in the CSR.

3. Read the CSR and obtain the failed address. If CSR bit 14 equals 0, then bits A11-A17 are loaded into CSR bits 5-11. If CSR bit 14 equals 1, then bits A18-21 have been loaded into CSR bits 5-8. Bit 2 is a read/write bit reset to zero on power-up or BUS INIT.

5-11 Error Address Bits. If a parity error occurs on a DATI or DATIO(B) cycle, then A11-A17 are stored in CSR bits 5-11 and bits A18-A21 are latched. The 18-bit address machines require only one read of the CSR to obtain the failed address. The CSR bit 14 set to 0 allows the logic to pass A11-A17 to the LSI-11 Bus. A 22-bit machine requires two reads. The first read (with CSR bit-14 set to 0) sends contents to CSR bits 5-11. Then the software must set CSR bit-14 equal to 1 to enable A18-21 to be read from CSR bits 5-8.

The parity error address locates a parity error to a 1K segment of memory. These are read/write bits and are not reset to zero via power-up or BUS INIT. If a second parity error is found, the new failed address will be stored in the CSR.

14 Extended CSR Read Enable. For a functional description of what this bit does, refer to the preceeding Error Address description.

1. Bit 14=0; always for 128K word machine.

2. Bit 14=0; first read on 2048K word machine.

3. Bit 14=1; second read on 2048K word machine.

15 Parity Error. When set, this bit indicates that a parity error has occurred. The bit lights a red LED on the module, providing visual indication of a parity error. Bit 15 is a read/write bit. It is reset to zero via power-up or by BUS INIT. It will remain set unless rewritten or initialized.

3.5.4.2 Parity Error LED

The PM-SV128 memory contains one RED light emitting diode (LED), CR1, that is visible when the memory is installed in a backplane. If the LED is illuminated, it indicates that a parity error was detected during a memory read operation. If bit 0 of the CSR is set at the time the parity error occurred, the memory will cause the processor to trap through the parity error trap vector, location 114. The LED will remain illuminated until the system executes a BUS RESET or the software resets bit 15 of the CSR.

3.5.5 SWITCH SETTINGS

The PM-SV128 memory board is designed to mechanically fit into the DEC LSI-11 series computers. The board occupies the space required by one standard DEC dual-wide printed circuit board and may be installed into any Q-bus slot (18 bit addressing) or any extended Q-bus (EQB) slot (22 bit addressing).

Starting and Ending Addresses

NOTE: ALPHABETICAL NOTATION A, B, C .... "JUMPER IN" = CONNECTION TO GROUND. DAISY CHAIN FASHION IS NECESSARY FOR MULTIPLE GROUND CONNECTION

1 = ON = JUMPER IN
0 = OFF = JUMPER OUT

MEMORY SIZE (IN KBYTES)	STARTING ADDRESS A	B	C	D	2	3	4	5	E	10	ENDING ADDRESS G	H	I	J	9	E	7	8	K
0-128	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	0	0	0	0
0-256	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	0	0	0
128-256	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0
256-512	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	0	0	0
512-768	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	0	1	0	0
768-1024	1	1	1	1	1	0	1	0	0	0	1	1	1	1	1	1	1	0	0
1024-1280	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	1	0
1280-1536	1	1	1	1	1	0	0	1	0	0	1	1	1	1	1	1	0	1	0
1536-1792	1	1	1	1	1	1	0	1	0	0	1	1	1	1	1	0	1	1	0
1792-2048	1	1	1	1	1	0	1	1	0	0	1	1	1	1	1	1	1	1	0
2048-2304	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	0	0	0	1
2304-2560	1	1	1	1	1	0	0	0	1	0	1	1	1	1	1	1	0	0	1
2560-2816	1	1	1	1	1	1	0	0	1	0	1	1	1	1	1	0	1	0	1
2816-3072	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	0	1
3072-3328	1	1	1	1	1	1	1	0	1	0	1	1	1	1	1	0	0	1	1
3328-3584	1	1	1	1	1	0	0	1	1	0	1	1	1	1	1	1	0	1	1
3584-3840	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1	0	1	1	1
3840-4096	1	1	1	1	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1

Starting and Ending Addresses Within 0-256KB

ADDRESS (IN KBYTES)	A	B	C	D	2	3	4	5	E	10
7	1	1	1	1	1	1	1	1	0	1
8	0	0	0	0	0	0	0	0	0	0
16	1	0	0	0	0	0	0	0	0	0
24	0	1	0	0	0	0	0	0	0	0
32	1	1	0	0	0	0	0	0	0	0
40	0	0	1	0	0	0	0	0	0	0
48	1	0	1	0	0	0	0	0	0	0
56	0	1	1	0	0	0	0	0	0	0
64	1	1	1	0	0	0	0	0	0	0
72	0	0	0	1	0	0	0	0	0	0
80	1	0	0	1	0	0	0	0	0	0
88	0	1	0	1	0	0	0	0	0	0
96	1	1	0	1	0	0	0	0	0	0
104	0	0	1	1	0	0	0	0	0	0
112	1	0	1	1	0	0	0	0	0	0
120	0	1	1	1	0	0	0	0	0	0
128	1	1	1	1	0	0	0	0	0	0
136	0	0	0	0	1	0	0	0	0	0
144	1	0	0	0	1	0	0	0	0	0
152	0	1	0	0	1	0	0	0	0	0
160	1	1	0	0	1	0	0	0	0	0
168	0	0	1	0	1	0	0	0	0	0
176	1	0	1	0	1	0	0	0	0	0
184	0	1	1	0	1	0	0	0	0	0
192	1	1	1	0	1	0	0	0	0	0
200	0	0	0	1	1	0	0	0	0	0
208	1	0	0	1	1	0	0	0	0	0
216	0	1	0	1	1	0	0	0	0	0
224	1	1	0	1	1	0	0	0	0	0
232	0	0	1	1	1	0	0	0	0	0
240	1	0	1	1	1	0	0	0	0	0
248	0	1	1	1	1	0	0	0	0	0
256	1	1	1	1	1	0	0	0	0	0
	G	H	I	J	9	6	7	8	K	

1 = ON = JUMPER TO GROUND
0 = OFF = JUMPER OUT

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Parity Control Register Selection

CSR SELECTION (FOR -1Ø Ø -1Ø1 ONLY)				
NO. OF CSR IN SYSTEM	POSITION (S1) 1	2	3	4
1 ST	1	1	1	1
2 ND	0	1	1	1
3 RD	1	0	1	1
4 TH	0	0	1	1
5 TH	1	1	0	1
6 TH	0	1	0	1
7 TH	1	0	0	1
8 TH	0	0	0	1
9 TH	1	1	1	0
10 TH	0	1	1	0
11 TH	1	0	1	0
12 TH	0	0	1	0
13 TH	1	1	0	0
14 TH	0	1	0	0
15 TH	1	0	0	0
16 TH	0	0	0	0
0 = OFF POSITION 1 = ON POSITION				

Jumpers on the SV128 memory:

22-bit parity
18-bit addressing parity W3 IN, W4 OUT (Factory Standard)
22-bit addressing parity W3 OUT, W4 IN

I/O page select:

Standard I/O page W13 OUT, W14 IN (Factory Standard)
Reduced I/O page W13 IN, W14 OUT

Battery backup. (Plessey does not support battery backup.)

Enabled W15 IN, W16 OUT (Factory Standard)
Disabled W15 OUT, W16 IN

Other factory set jumpers:

W1 IN W9 IN
W2 OUT W10 OUT
W5 IN W11 OUT
W6 OUT W12 IN
W7 IN
W8 OUT

3.5.6 MEMORY SPECIFICATIONS

Refer to Table 3-3 for specifications of the PM-SV128 memory.