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Table 3-11. Standard PM-DLV11J Configuration

Channel	Address	Register	Vector
1	176500	RCSR1	300
	176502	RBUF1	
	176504	XCSR1	304
	176506	XBUF1	
2	176510	RCSR2	310
	176512	RBUF2	
	176514	XCSR2	314
	176516	XBUF2	
3	176520	RCSR3	320
	176522	RBUF3	
	176524	XCSR3	324
	176526	XBUF3	
4	176530	RCSR4	330
	176532	RBUF4	
	176534	XCSR4	334
	176534	XBUF4	
2			

Baud Rate: Channel 1 thru 4 9600
 Break Response: None
 UART Operation: 8 data bits; no parity; one stop bit
 Serial Interface: EIA RS232C

If the board is to be reconfigured for special needs, use Figure 3-5 as a guide to jumper and pad locations.

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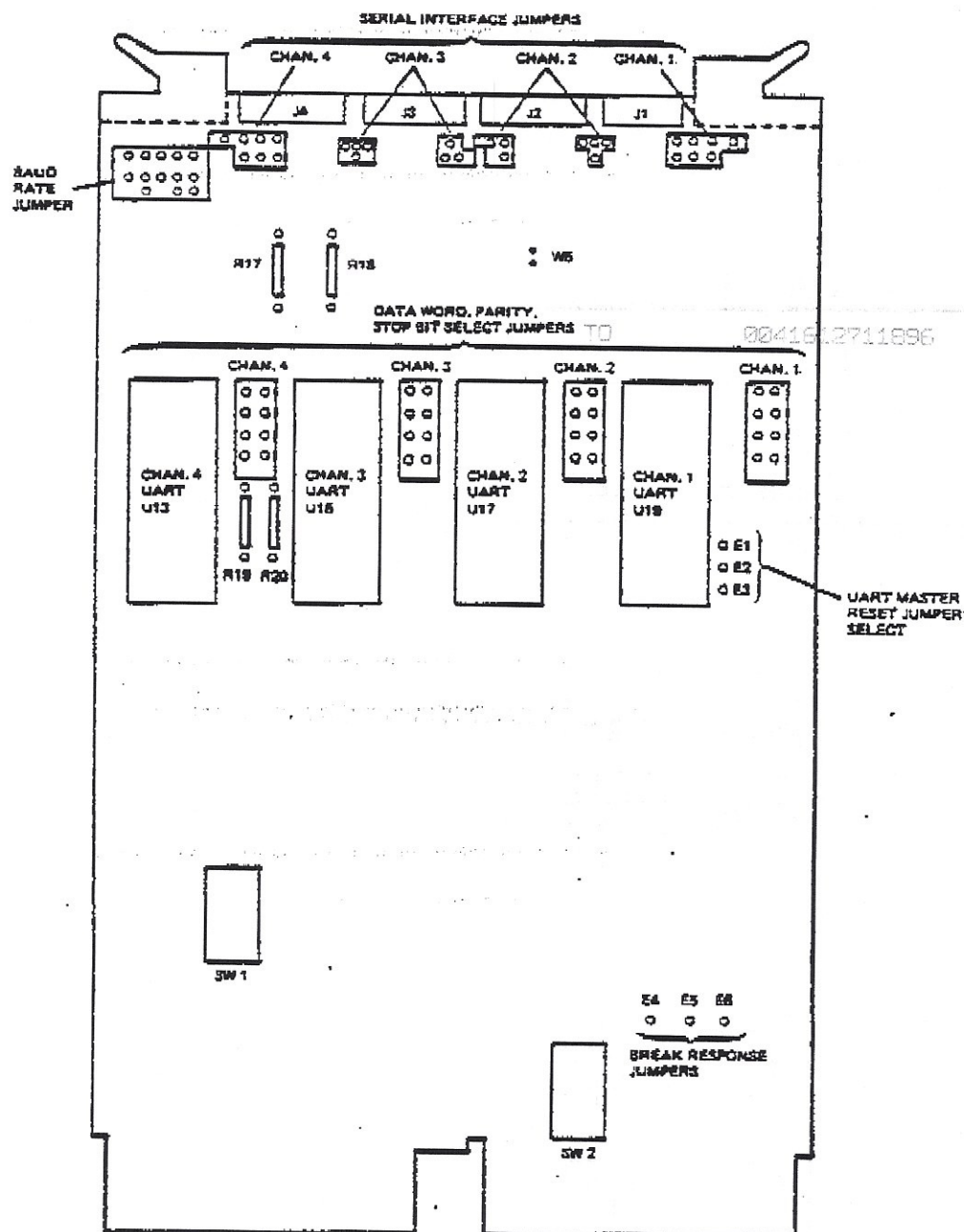


Figure 3-5. PM-DLV11J Jumper and Pad Locations

Switches are configured to establish the base address (BA) for the module. This base address is the channel 0 RCSR address. The device

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address format is shown in Figure 3-5. The remaining device addresses follow through a total of 16 contiguous word addresses; however, it is possible to independently dedicate the last four addresses (channel 4) to a console device. When configured for console device operation, the channel's device register addresses will be 177560-177566. However, since the MFV11 Multifunction board has the console device, the Channel 4 on the PM-DLV11J should not be set as the console.

3.11.3.1 Switch Definitions

SW1-1 Unused
SW1-2 Unused

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(J4) Regular Port Console

SW1-3 ON OFF
SW1-4 OFF ON

	<u>Vector</u>	<u>300</u>	<u>340</u>	<u>400</u>	<u>440</u>
SW1-5	bit 5	ON	OFF	ON	OFF
SW1-6	bit 6	OFF	OFF	ON	ON
SW1-7	bit 7	OFF	OFF	ON	ON
SW1-8	bit 8	ON	ON	OFF	OFF

<u>Address</u>	<u>176500</u>	<u>176540</u>	<u>176600</u>	<u>176640</u>
S2-1 bit 5	ON	OFF	ON	OFF
S2-2 bit 6	OFF	OFF	ON	ON
S2-3 bit 7	ON	ON	OFF	OFF
S2-4 bit 8	OFF	OFF	OFF	OFF
S2-5 bit 9	ON	ON	ON	ON
S2-6 bit 10	OFF	OFF	OFF	OFF
S2-7 bit 11	OFF	OFF	OFF	OFF
S2-8 bit 12	OFF	OFF	OFF	OFF

The baud rate of each port may be changed by wirewrapping the wirewrap pin for that channel to the clock speed. Factory settings are pins 1,2,3,4 wirewrapped to pin F, which means 9600 baud. The transmit and receive speed are tied together.

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Baud Rate (1,2,3,4)

150=B
300=G
600=C
1200=A
2400=D
4800=E
9600=F
19.2K=J
38.4K=H

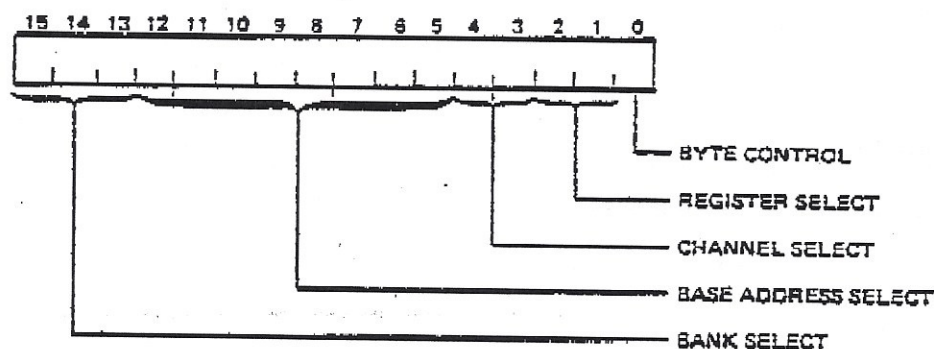
Standard Factory:

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PM-DLV11J	J1	J2	J3	J4
Baud Rate:	9600	9600	9600	9600
Data Bits:	8	8	8	8
Stop Bits:	1	1	1	1
Parity:	none	none	none	none
Address:	776500	776510	776520	776530

3.11.4 ADDRESS SELECTION

If channel 4 is configured as a printer port, its device address will be 177514 for the Transmitter Control/Status Register (XCSR) and 177516 for the Transmitter Buffer (XBUF). The device address format is shown below.



The base address is selected by switch S2. Channel and register select bits are set as shown in Table 3-12. These bits are not switch selectable, but are decoded automatically by the PM-DLV11J logic.

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Table 3-12. Channel and Register Selection

Channel Select			Register Select		
Channel	Bit 4	Bit 3	Register	Bit 2	Bit 1
1	0	0	RCSR	0	0
2	0	1	RBUF	0	1
3	1	0	XCSR	1	0
4	1	1	XBUF	1	1

Address Format

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The PM-DLV11J responds to any address in the upper 4K peripheral page. It is limited to blocks of 16 addresses that start at addresses whose last two digits are either 00 or 40. If channel 4 is used as the console device, 12 slot memory blocks started at XXXX00 or XXXX40 may be used. Each channel has four device registers that may be individually addressed by a program. The device registers are as follows:

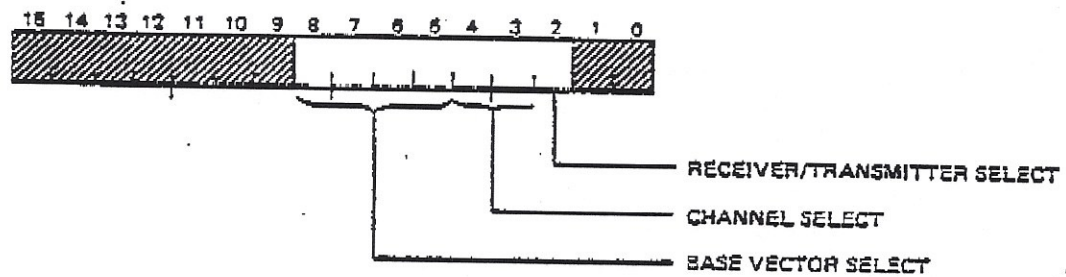
Receiver Control/Status Register	(RCSR)
Receiver Buffer	(RBUF)
Transmitter Control/Status Register	(XCSR)
Transmitter Buffer	(XBUF)

If channel 4 is configured as a dedicated console interface, its device register addresses will be 177560 thru 177566.

3.11.5 VECTOR FORMAT

Eight interrupt vectors are switch and PROM selected on PM-DLV11J. Each channel is capable of generating two interrupts, one from the receiver buffer, and one from the transmitter buffer. Vector address range from 000 to 776. The console device interrupt vectors are 60 and 64, printer port vector is 200. If an interrupt acknowledge is granted, the vector address is placed on the data/address bus lines. The format for the vector address follows.

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The base vector is selected by switch S1. See Table 3-13. P.12/24

Table 3-13. Vector Address Bit Switches

Vector Address Bit	Switch
8	S1-8
7	S1-7
6	S1-6
5	S1-5

The channel select bits are PROM, not switch selected. They are decoded as shown in Table 3-14.

Table 3-14. Vector Channel Select

Channel	Bit 4	Bit 3
1	0	0
2	0	1
3	1	0
4	1	1

The receiver/transmitter select bit is decoded as follows:

0 = Receiver

1 = Transmitter

This bit is not switch selectable, but is set automatically by the PM-DLV11J.